

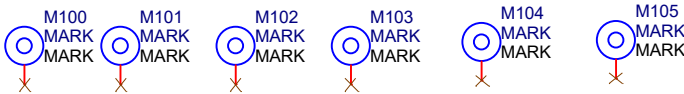
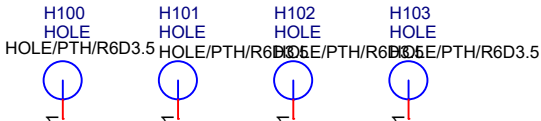
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## 6 LAYERS PCB STACK é g PCB=1.6mm

TOP	Prepreg 1080*1 (75um)	Silkscreen Q5um 1oz (35um)
GND1	Prepreg 2116*1 (115um)	Hoz (18um)
POWER	Adjust Core Ø65um	Hoz (18um)
SIGNAL	Prepreg 2116*1 (115um)	Hoz (18um)
GND2	Prepreg 1080*1 (75um)	Hoz (18um)
BOTTOM		1oz (35um) Silkscreen Q5um

Note:  
器件参数说明  
1:如果 Value 为 DR,说明暂时不贴。  
2:如果 Option 有 DR,说明预留先不贴。

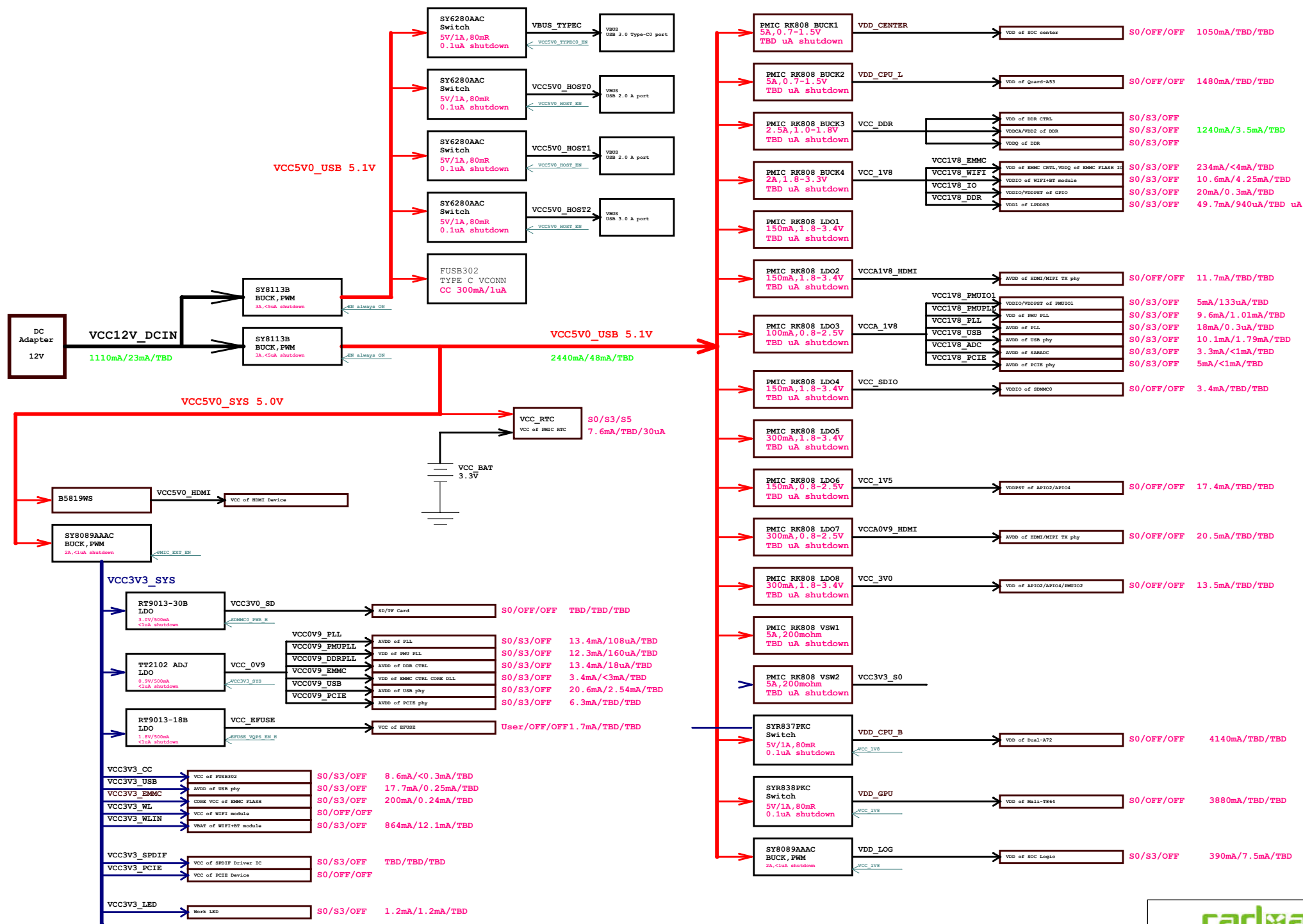


Size	Title: <b>ROCK Pi 4 Plus</b>	REV
A4	Page Name: <b>Index</b>	1.72
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Change List

Version	Date	Author	Change Note	Approved
V1.0	201708	Charlie	First edition	

## RK3399 POWER DIAGRAM



# I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK808	0x1b	PMIC	100kHz, 400KHz
					SYR837PKC	0x40	DC-DC BUCK	100kHz, 400KHz, 3.4MHz
					SYR838PKC	0x41	DC-DC BUCK	100kHz, 400KHz, 3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5		VCC_1V8			Low Speed CONNECTOR	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_HDMI I2C_SCL_HDMI	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_MEMS I2C_SCL_MEMS	VCC_1V8	Fairchild FUSB302B	0x44, 0x46	USB-TypeC Mux	100kHz, 400KHz, 1MHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2		VCC_1V8			Low Speed CONNECTOR	
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	



Size	Title: <b>ROCK Pi 4 Plus</b>	REV
A4	Page Name: <b>I2C Map</b>	1.72
Date: <b>Tuesday, August 03, 2021</b> Sheet <b>4</b> of <b>26</b>		

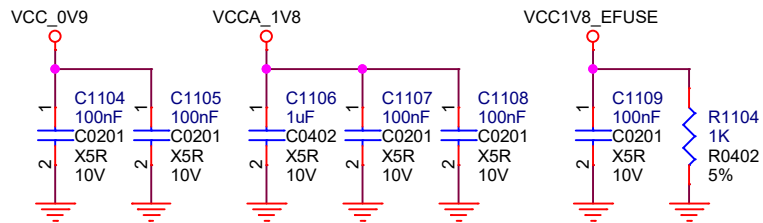
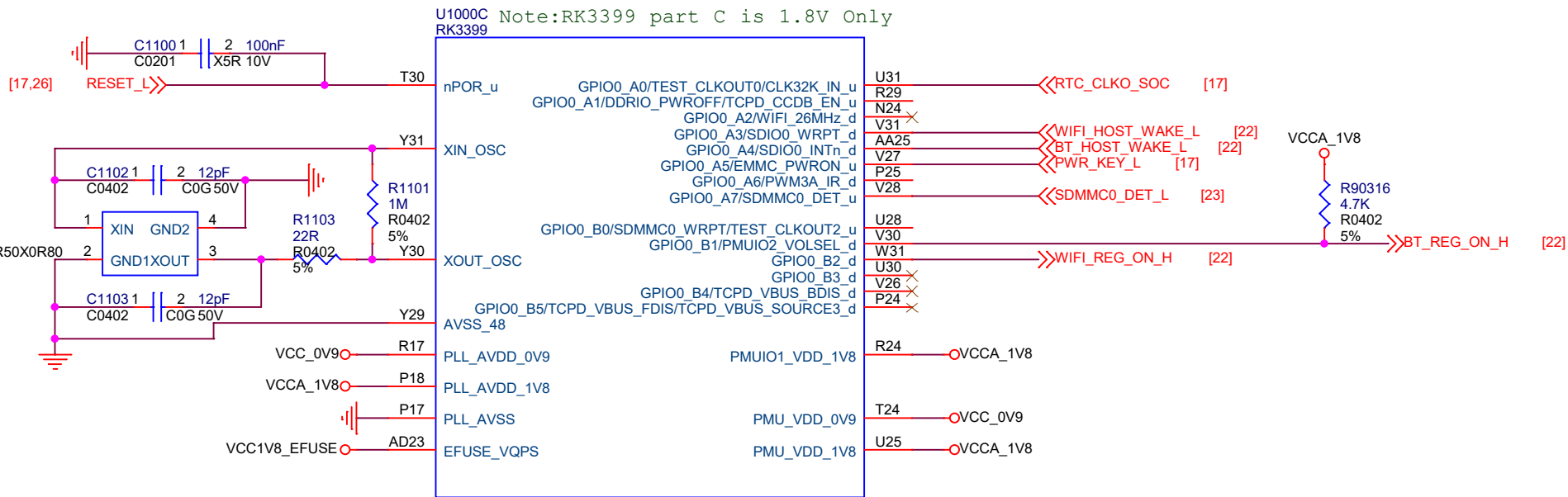
# Power Domain Map

Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuiol_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLDO3
Part E	PMUIO2	pmul830_gpio1abcd	1.8V (Default) 3.0V	VCC_1V8	RK808-D Buck4
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_SYS	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V (Default) 3.0V	VCC_1V8	RK808-D VLDO3
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V (Default)	VCC_1V5 VCC_3V0	RK808-D VLDO6 RK808-D VLDO8
Part J	APIO5	audio_gpio3d_gpio4a	1.8V (Default) 3.0V	VCC_1V8	RK808-D Buck4
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V (Default)	VCC_SDIO	RK808-D VLDO4

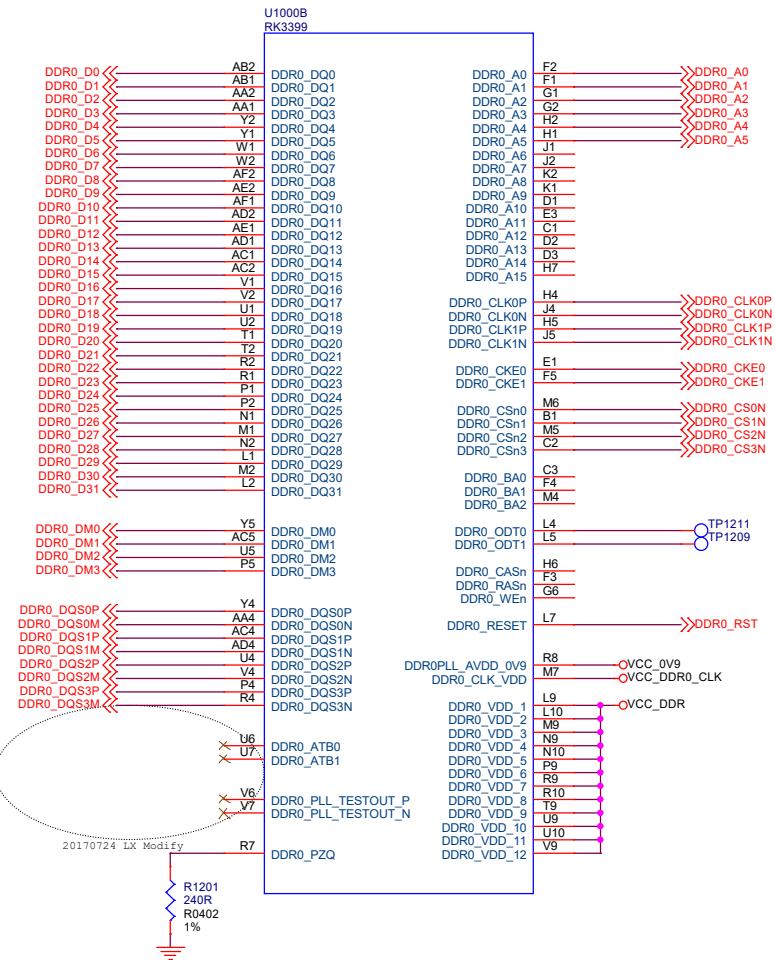
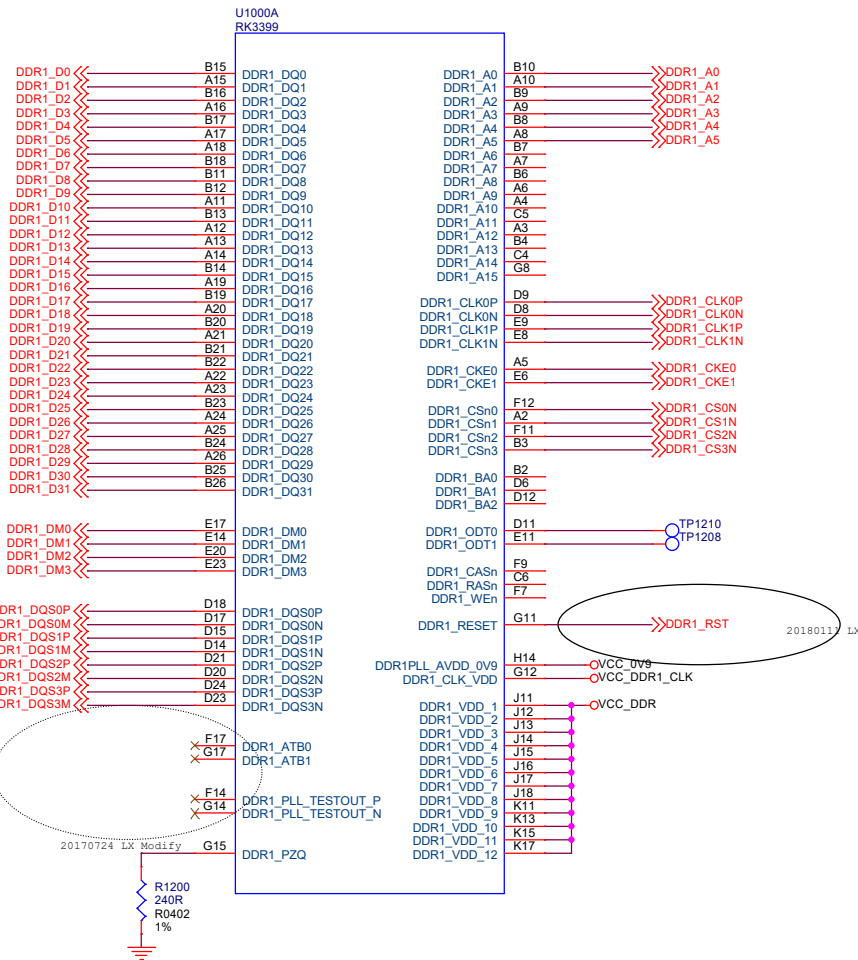


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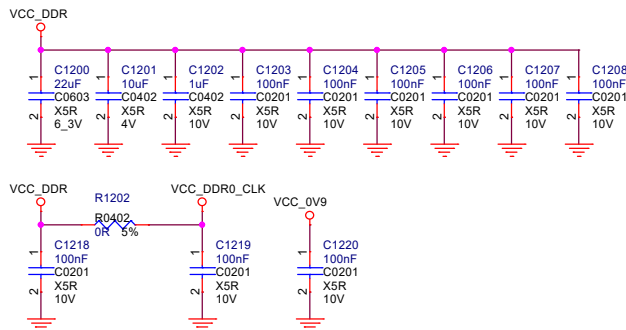


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A4	Page Name: <b>RK3399 PMU Controller</b>	1.72
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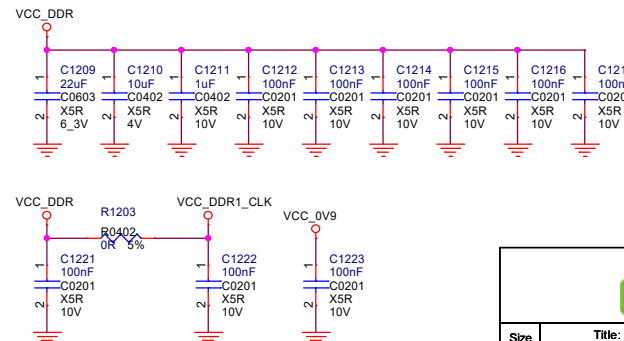
## DDR FILTER

Note:R1202 cannot be deleted



## DDR FILTER

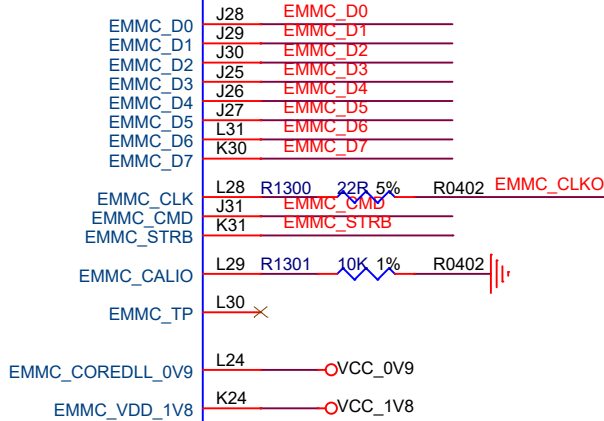
Note:R1203 cannot be deleted



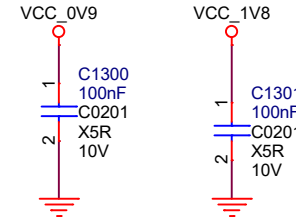
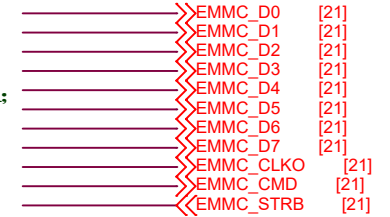
radxa



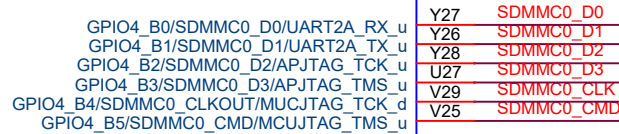
U1000H  
RK3399



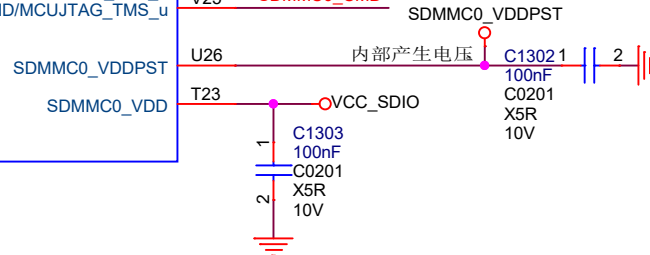
EMMC design rule:  
1. Data[0:7], cmd strobe 做为一组, 并行走线并包地, 组内等长要求为  $\pm 100\text{mil}$ ;  
2. Clk 需要单独走线并包地处理, 与 data 间的延时小于  $20\text{ps}$ ;  
3. Max trace length  $< 3.93\text{ inches}$ ;  
4. Trace impedance  $50\text{ohm} \pm 10\%$ ;  
5. 与其他信号间距遵循原则;  
6. R1300 靠近 S 的位置;

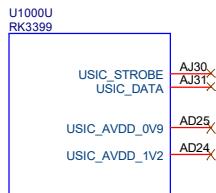


U1000F  
RK3399

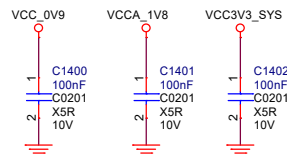
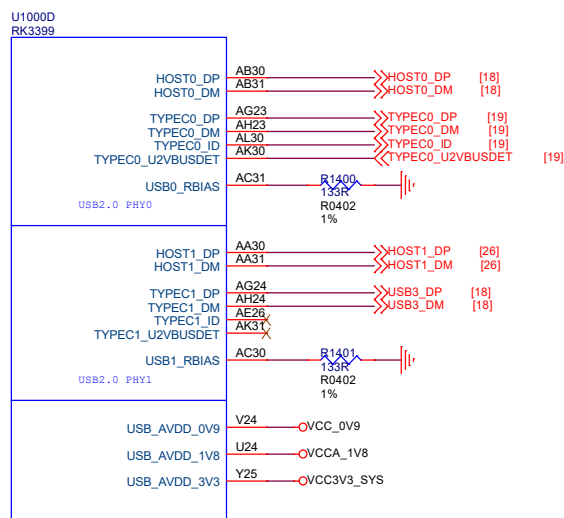


SDMMC design rule:  
1. Data[0:3], cmd 做为一组, 并行走线并包地, 组内等长要求为  $\pm 100\text{mil}$ ;  
2. Clk 需要单独走线并包地处理, 与 data 间的延时小于  $20\text{ps}$ ;  
3. Max trace length  $< 3.93\text{ inches}$ ;  
4. Trace impedance  $50\text{ohm} \pm 10\%$ ;  
5. 与其他信号间距遵循原则;



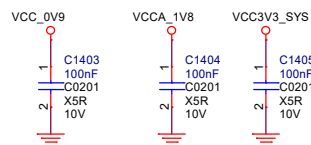
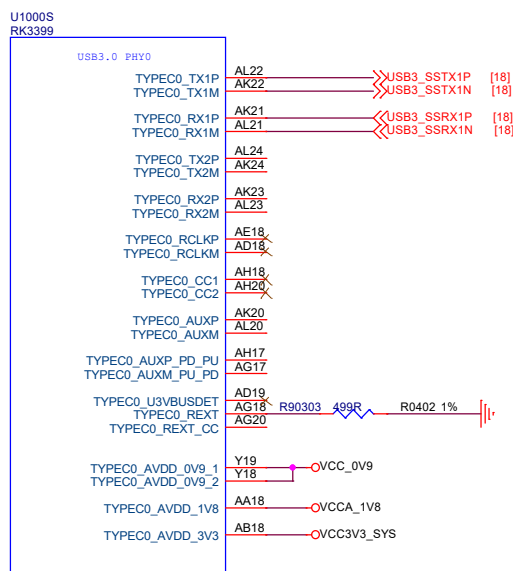


## USB2.0



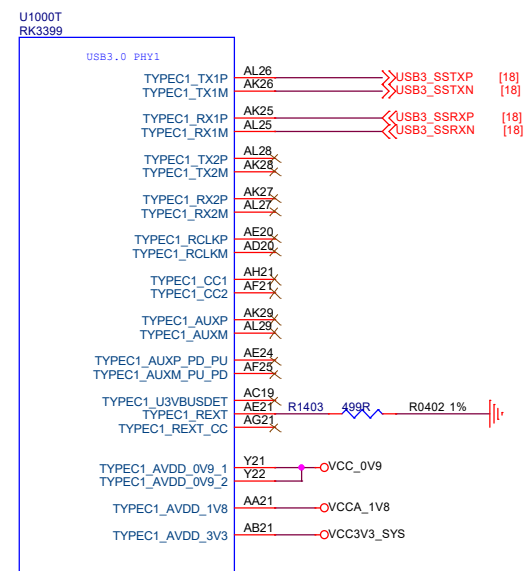
USB2.0 design rule:  
 1.Max intra-pair skew < 4 ps;  
 2.Max trace length < 6 inchs;  
 3.Max allowed via < 6;  
 4.Trace impedance 90ohm+/-10%;  
 5. 与其他信号间距遵循0原则 ;

## USB3.0



USB3.0 design rule:  
 1.Max intra-pair skew < 4 ps;  
 2.Max length skew between TX and RX < 1.6 ns;  
 3.Max trace length < 6 inchs;  
 4.Max allowed via < 4;  
 5.Trace impedance 90ohm+/-10%;  
 6. 与其他信号间距遵循0原则 ;

DP design rule:  
 1.Max intra-pair skew < 4 ps;  
 2.Max trace length < 6 inchs;  
 3.Max allowed via < 4;  
 4.Trace impedance 90ohm+/-10%;  
 5. 与其他信号间距遵循0原则 ;

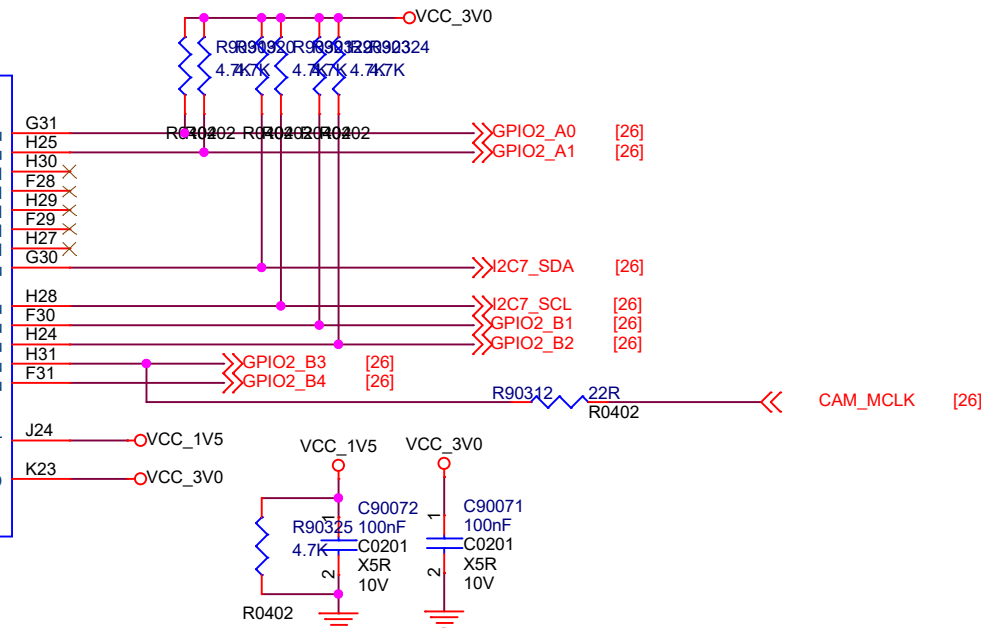




U1000L  
RK3399

GPIO2\_A0/VOP\_D0/CIF\_D0/I2C2\_SDA\_u  
GPIO2\_A1/VOP\_D1/CIF\_D1/I2C2\_SCL\_u  
GPIO2\_A2/VOP\_D2/CIF\_D2\_d  
GPIO2\_A3/VOP\_D3/CIF\_D3\_d  
GPIO2\_A4/VOP\_D4/CIF\_D4\_d  
GPIO2\_A5/VOP\_D5/CIF\_D5\_d  
GPIO2\_A6/VOP\_D6/CIF\_D6\_d  
GPIO2\_A7/VOP\_D7/CIF\_D7/I2C7\_SDA\_u  
  
GPIO2\_B0/VOP\_CLK/CIF\_VSYNC/I2C7\_SCL\_u  
GPIO2\_B1/SPI2\_RXD/CIF\_HREF/I2C6\_SDA\_u  
GPIO2\_B2/SPI2\_TXD/CIF\_CLKIN/I2C6\_SCL\_u  
GPIO2\_B3/SPI2\_CLK/VOP\_DEN/CIF\_CLKOUTA\_u  
GPIO2\_B4/SPI2\_CSn0\_u

APIO2\_VDDPST  
APIO2\_VDD



U1000R  
RK3399

MIPI\_RX0\_D0P AK15 << MIPI\_RX0\_D0P [26]  
MIPI\_RX0\_D0N AL15 << MIPI\_RX0\_D0N [26]  
  
MIPI\_RX0\_D1P AK14 << MIPI\_RX0\_D1P [26]  
MIPI\_RX0\_D1N AL14 << MIPI\_RX0\_D1N [26]  
  
MIPI\_RX0\_CLKP AK13 << MIPI\_RX0\_CLKP [26]  
MIPI\_RX0\_CLKN AL13 << MIPI\_RX0\_CLKN [26]  
  
MIPI\_RX0\_D2P AK12 << MIPI\_RX0\_D2P [26]  
MIPI\_RX0\_D2N AL12 << MIPI\_RX0\_D2N [26]  
  
MIPI\_RX0\_D3P AK11 << MIPI\_RX0\_D3P [26]  
MIPI\_RX0\_D3N AL11 << MIPI\_RX0\_D3N [26]  
  
MIPI\_RX0\_REXT AF14 R1600 4.02K%1 R0402 1%  
  
MIPI\_RX0\_AVDD\_1V8 AB14 VCC\_1V8

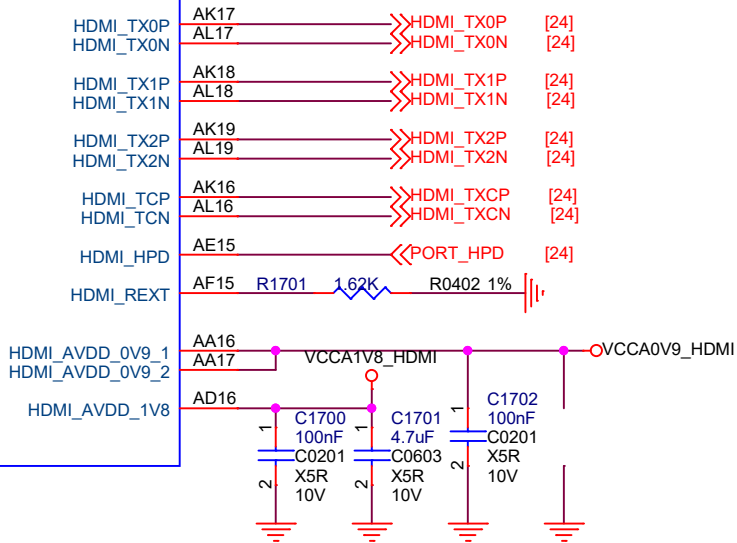
U1000P  
RK3399

MIPI\_TX1/RX1\_D0P AK6 << MIPI\_TX/RX\_D0P [26]  
MIPI\_TX1/RX1\_D0N AL6 << MIPI\_TX/RX\_D0N [26]  
  
MIPI\_TX1/RX1\_D1P AK7 << MIPI\_TX/RX\_D1P [26]  
MIPI\_TX1/RX1\_D1N AL7 << MIPI\_TX/RX\_D1N [26]  
  
MIPI\_TX1/RX1\_CLKP AK8 << MIPI\_TX/RX\_CLKP [26]  
MIPI\_TX1/RX1\_CLKN AL8 << MIPI\_TX/RX\_CLKN [26]  
  
MIPI\_TX1/RX1\_D2P AK9 << MIPI\_TX/RX\_D2P [26]  
MIPI\_TX1/RX1\_D2N AL9 << MIPI\_TX/RX\_D2N [26]  
  
MIPI\_TX1/RX1\_D3P AK10 << MIPI\_TX/RX\_D3P [26]  
MIPI\_TX1/RX1\_D3N AL10 << MIPI\_TX/RX\_D3N [26]  
  
MIPI\_TX1/RX1\_REXT AF11 R1601 4.02K%1 R0402 1%  
  
MIPI\_TX1/RX1\_AVDD\_1V8 AC10 VCC\_1V8

Dual  
MIPI  
Right



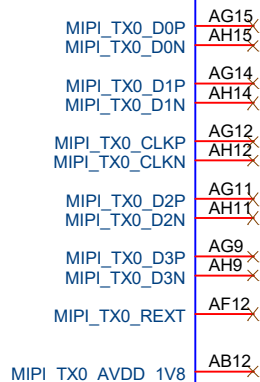
U1000N  
RK3399



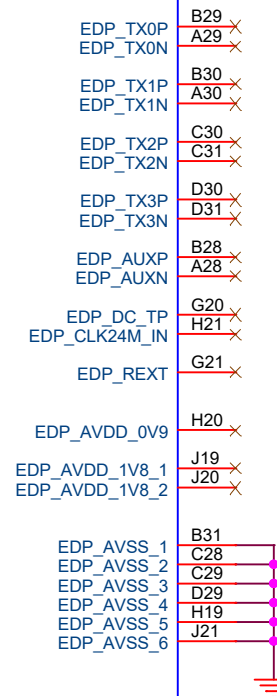
#### HDMI design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 80 ps;
- 3.Max trace length < 9.8 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
6. 与其他信号间距遵循原则 ;

U1000Q  
RK3399



U1000M  
RK3399



#### eDP design rule:

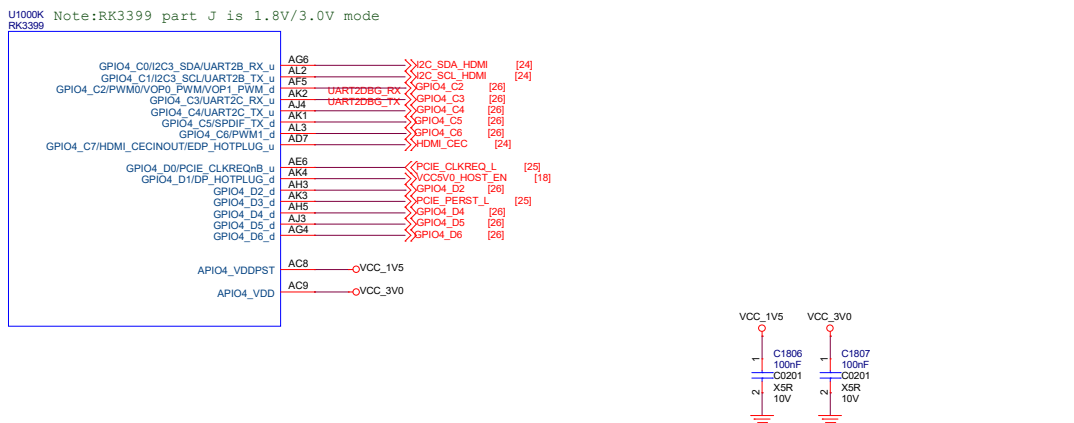
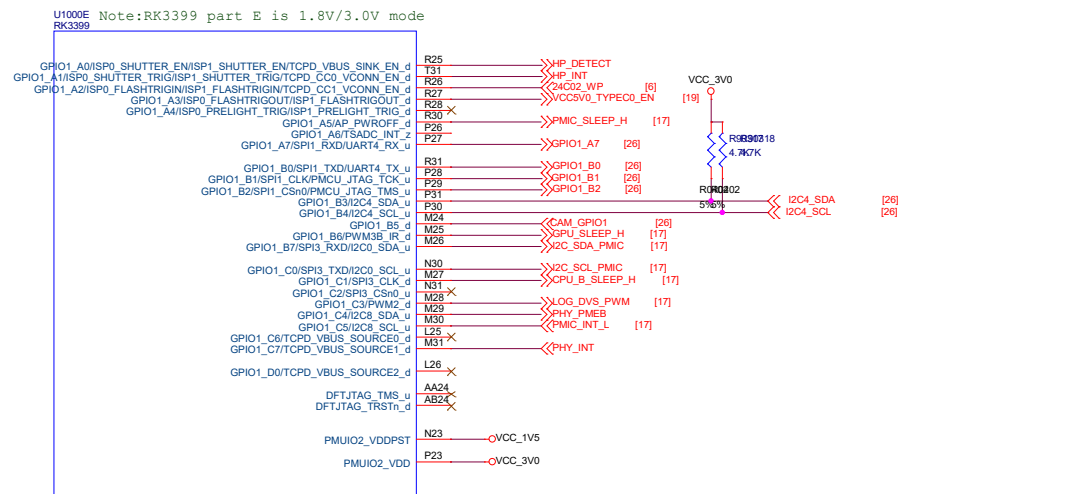
- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inches;
- 3.Max allowed via < 4;
- 4.Trace impedance 90ohm+/-10%;
5. 与其他信号间距遵循原则 ;

#### MIPI design rule:

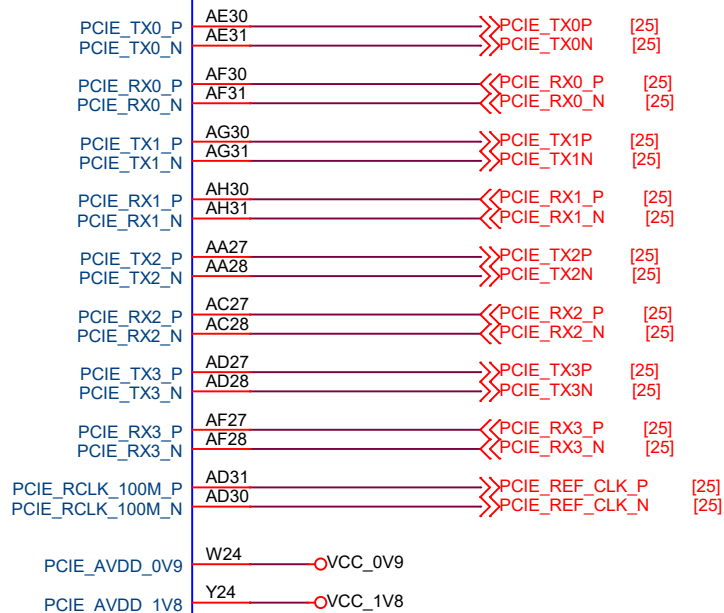
- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 7ps;
- 3.Max trace length < 7.2 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
6. 与其他信号间距遵循原则 ;



Size	Title: <b>ROCK Pi 4 Plus</b>	REV
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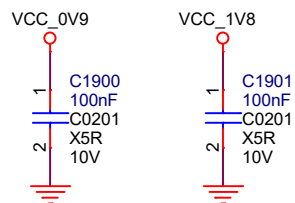


U10000  
RK3399



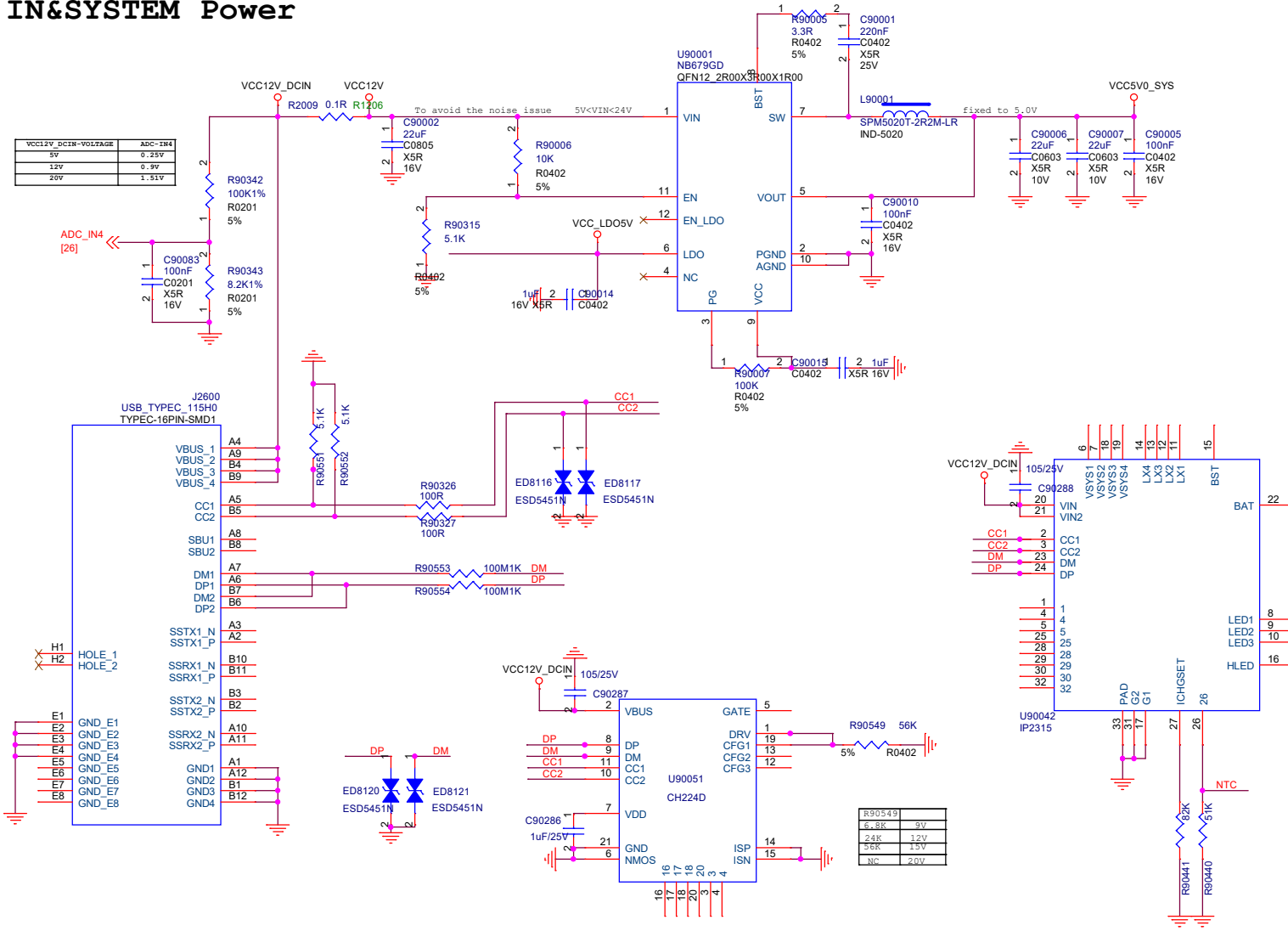
#### PCIE design rule:

1. Max intra-pair skew < 4ps;
2. Max inter-pair skew < 1.6 ns;
3. Max trace length < 14 inches;
4. Max allowed via < 4;
5. Trace impedance 100ohm+/-10%;
6. 与其他信号间距遵循原则；



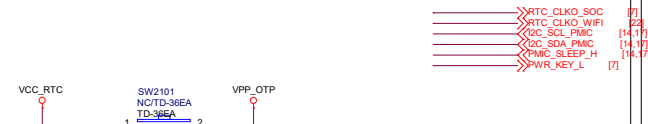
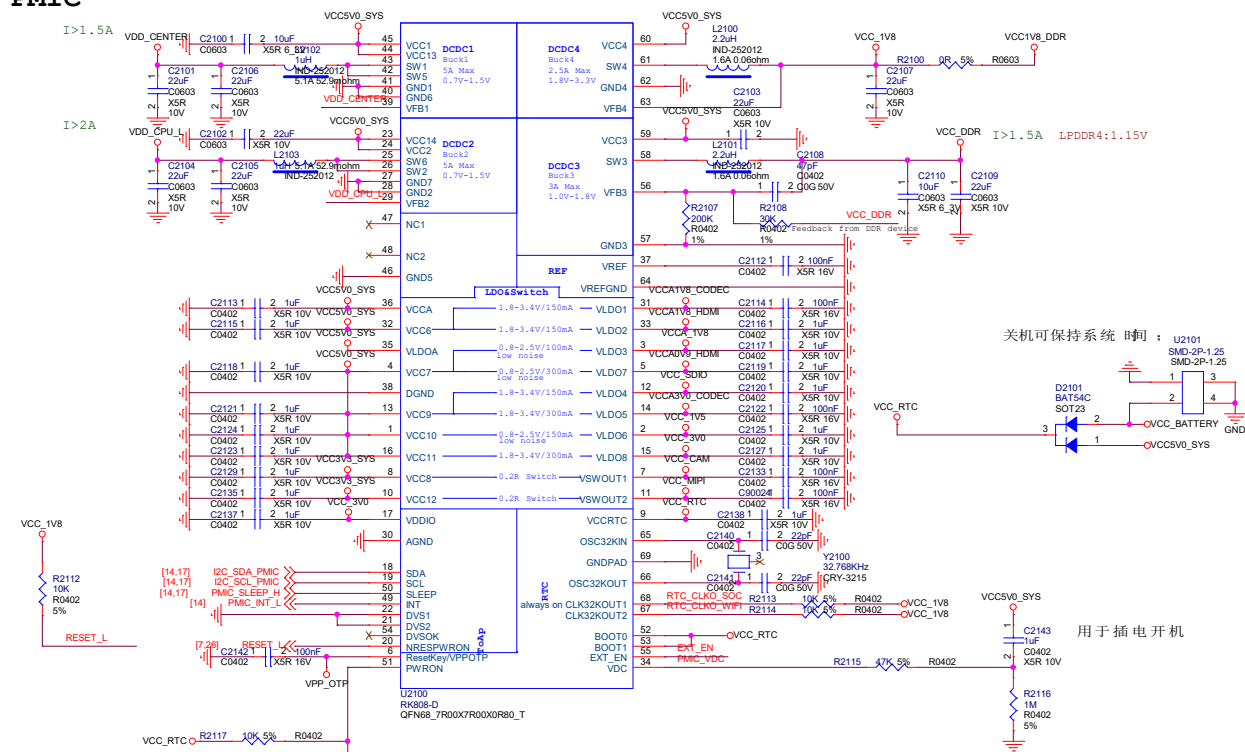
Size	Title: <b>ROCK Pi 4 Plus</b>	REV
A4	Page Name: <b>RK3399 PCIE</b>	1.72
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## DC IN&SYSTEM Power

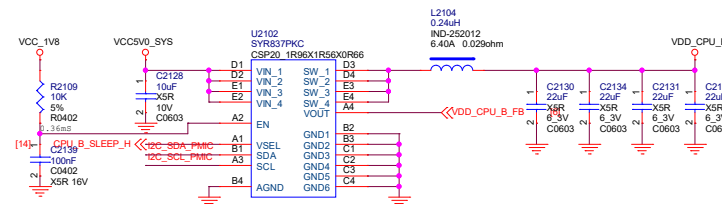




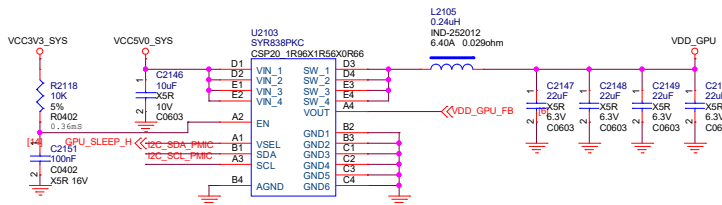
PMIC



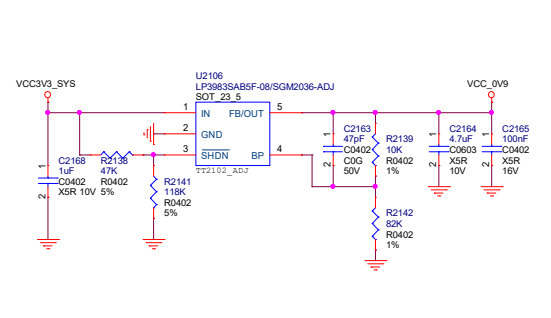
## VDD CPU B power



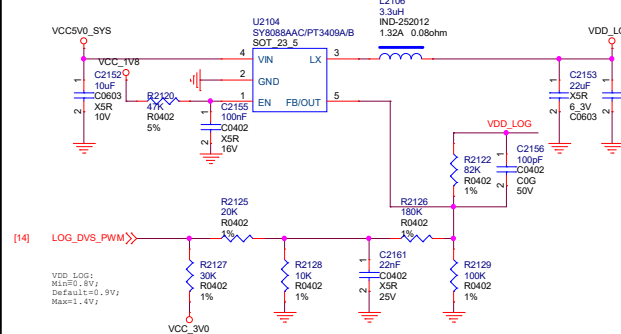
VDD GPU power



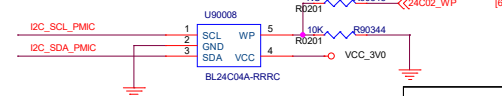
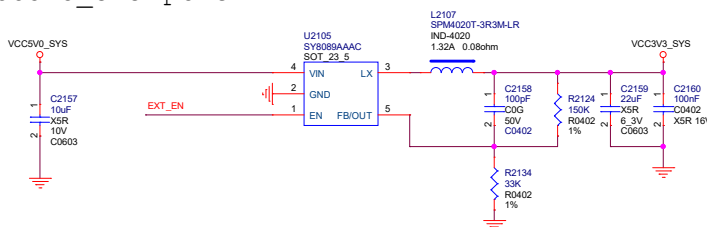
```
VCC 0V9 power
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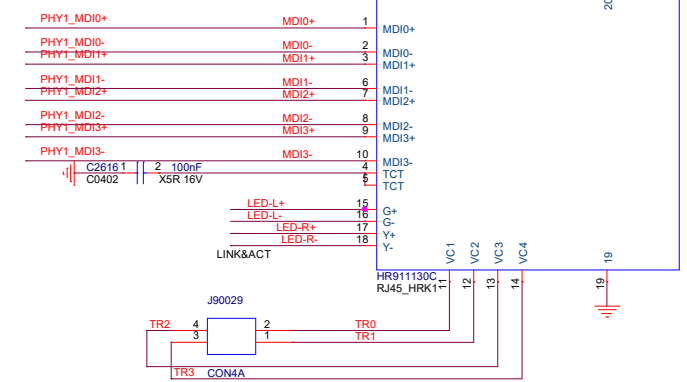
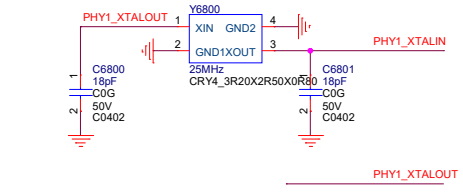


```
VDD LOG power
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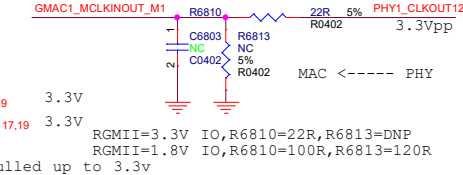


VCC3V3 SYS power

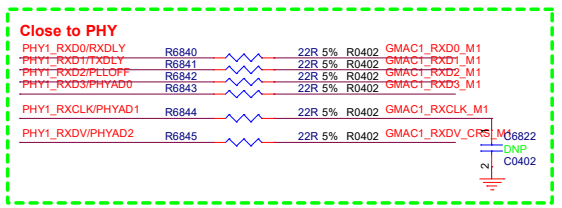
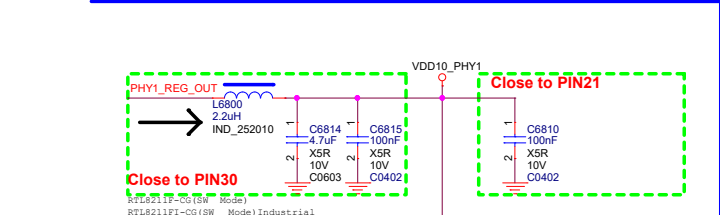
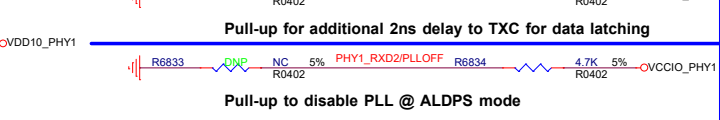
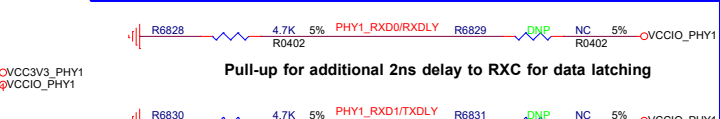
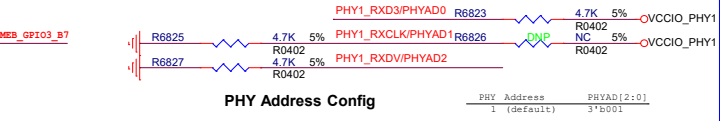
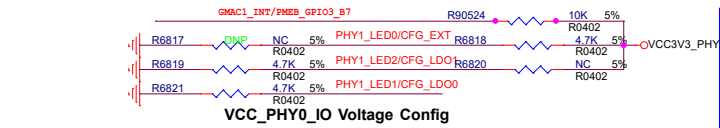
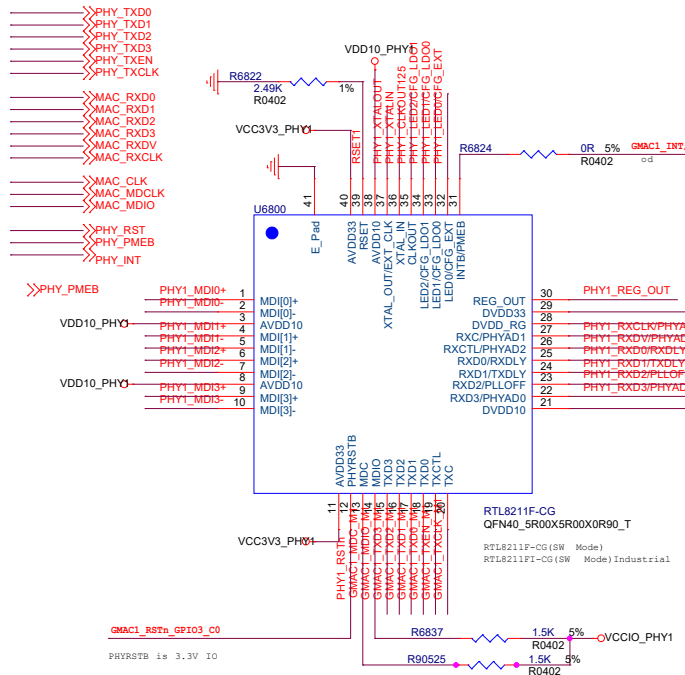




125M CLK FROM 8211 >>MAC\_CLK>>GMAC1\_MCLKINOUT\_M117  
>>MAC\_MDCLK>>GMAC1\_MDC\_M1 17  
>>MAC\_MDIO>>GMAC1\_MDIO\_M1 17  
  
>>PHY\_RST>>GMAC1\_RSTn\_GPIO3\_C0 17,19 3.3V  
>>PHY\_INT<<GMAC1\_INT/PMEB\_GPIO3\_B7 17,19 3.3V  
INT/PMEB INT OR WAKE UP LAN  
INT/PMEB need to connected with a 4.7k resistor and pulled up to 3.3V

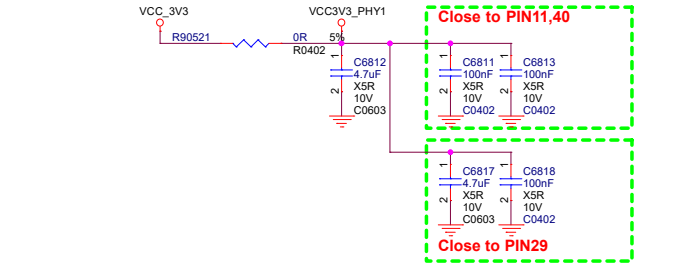
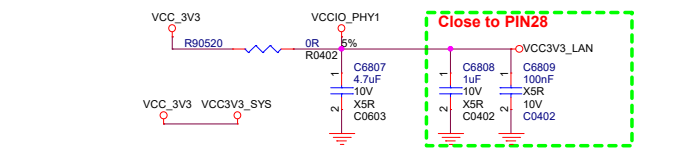
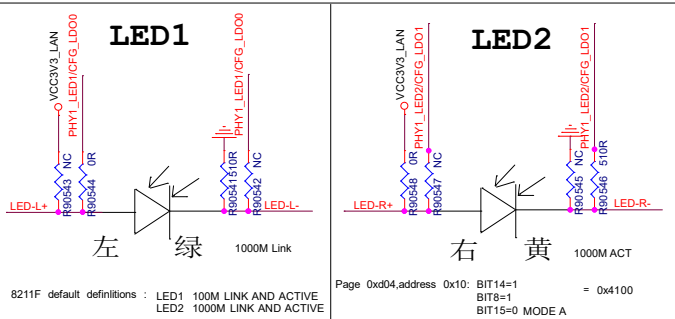


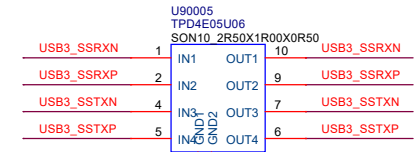
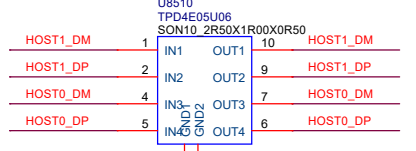
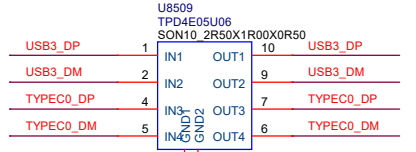
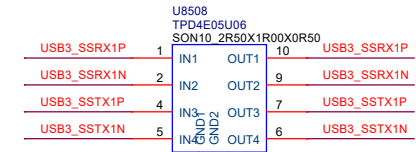
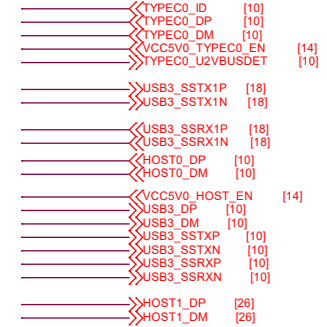
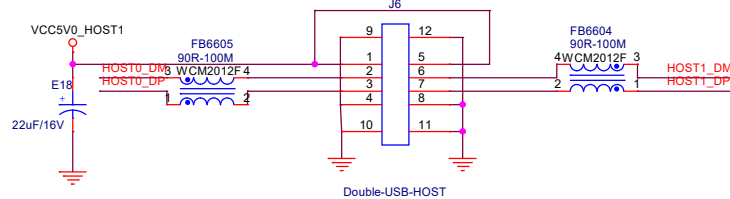
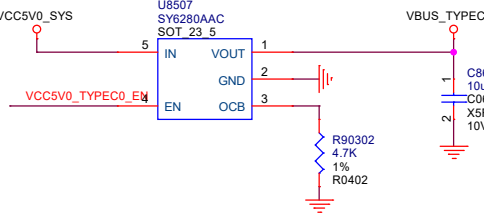
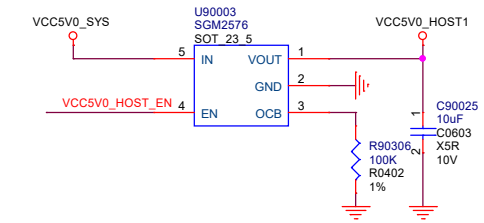
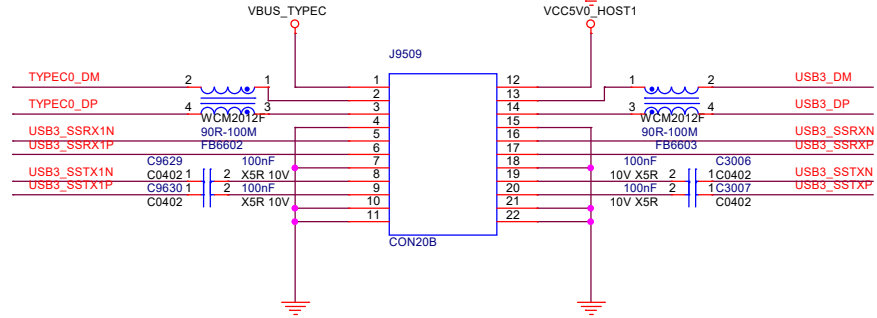
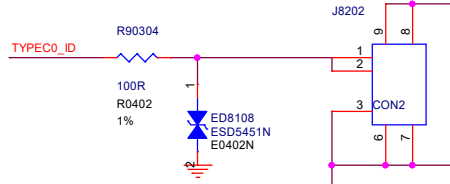
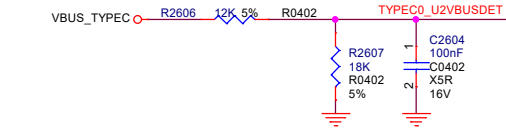
RGMII=3.3V IO,R6810=22R,R6813=DNP  
RGMII=1.8V IO,R6810=100R,R6813=120R

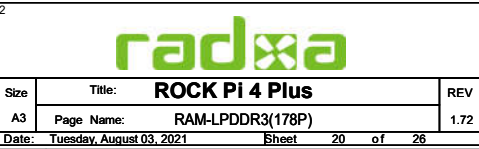


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RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V (default)	1'b1	2'b10
Internal 1.8V	1'b0	2'b10





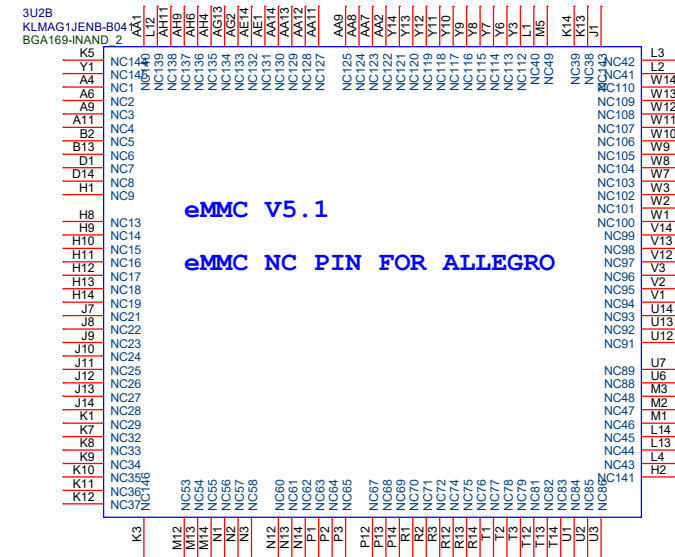
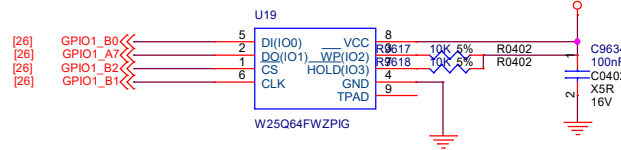
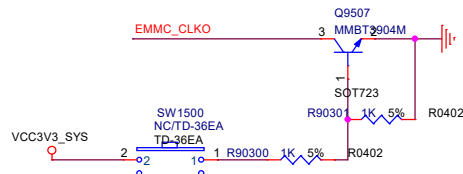
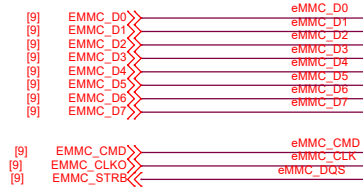
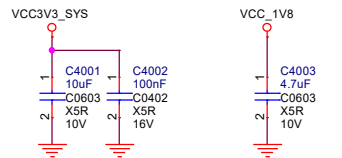
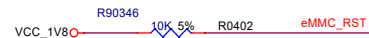
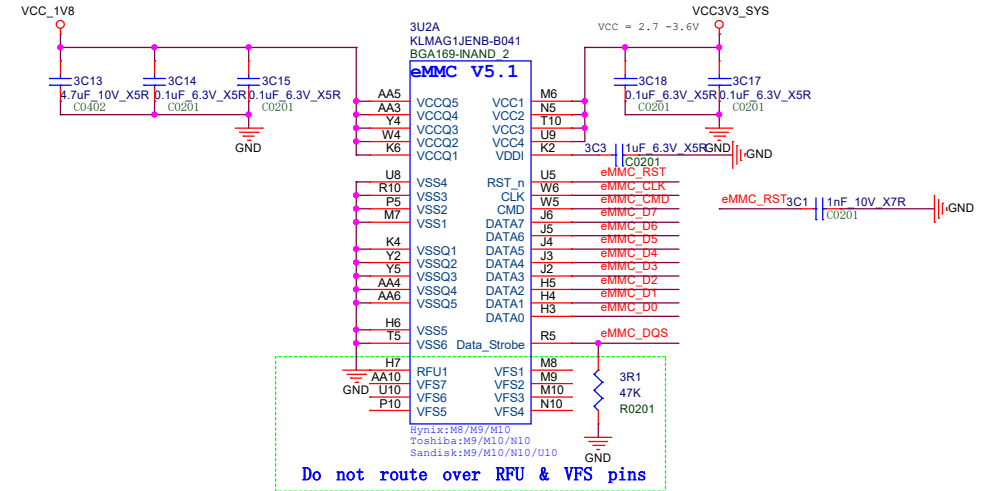


## eMMC FLASH



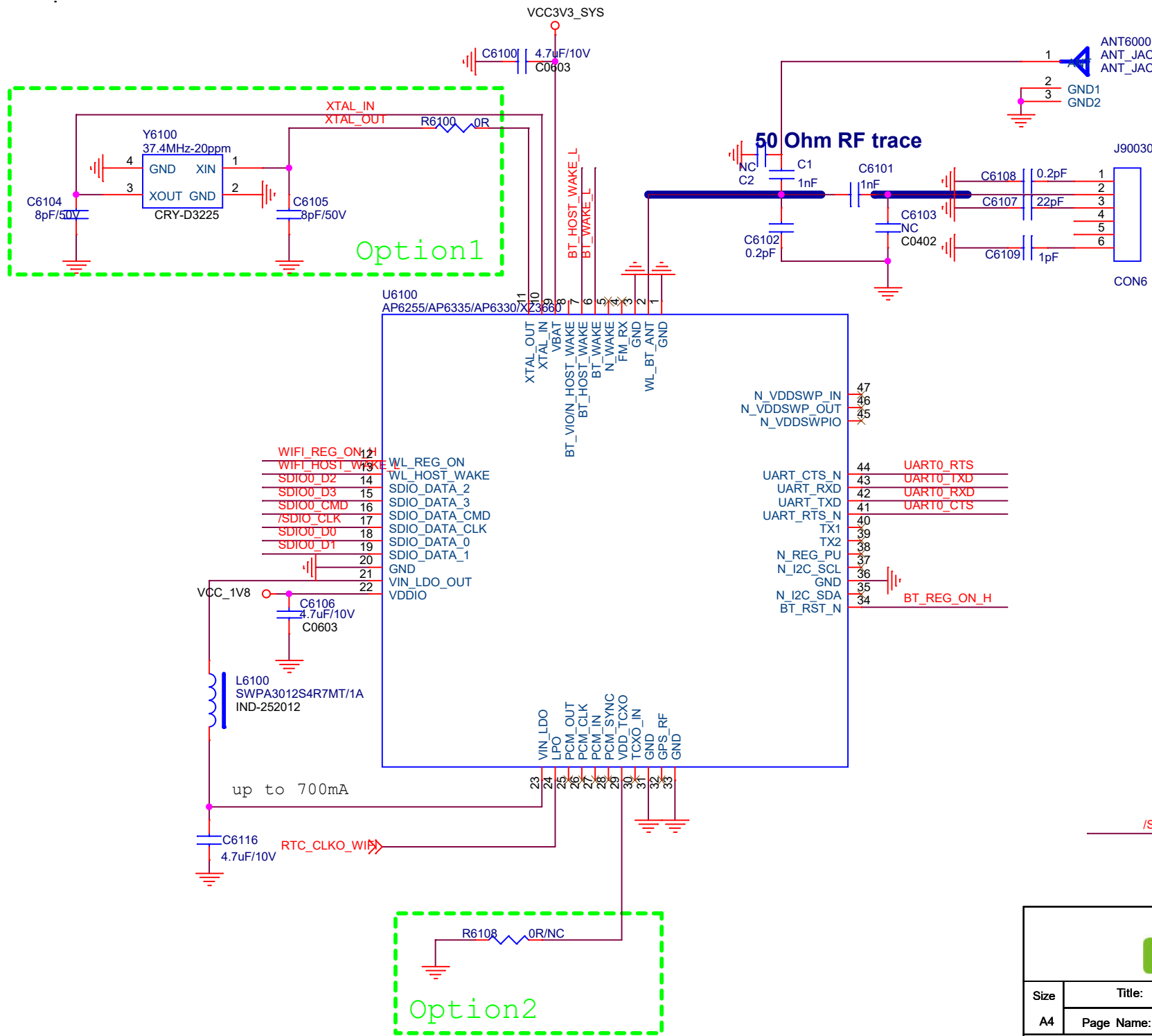
eMMC

PCB Decal:169pin balls Type(BGA)



eMMC V5.1

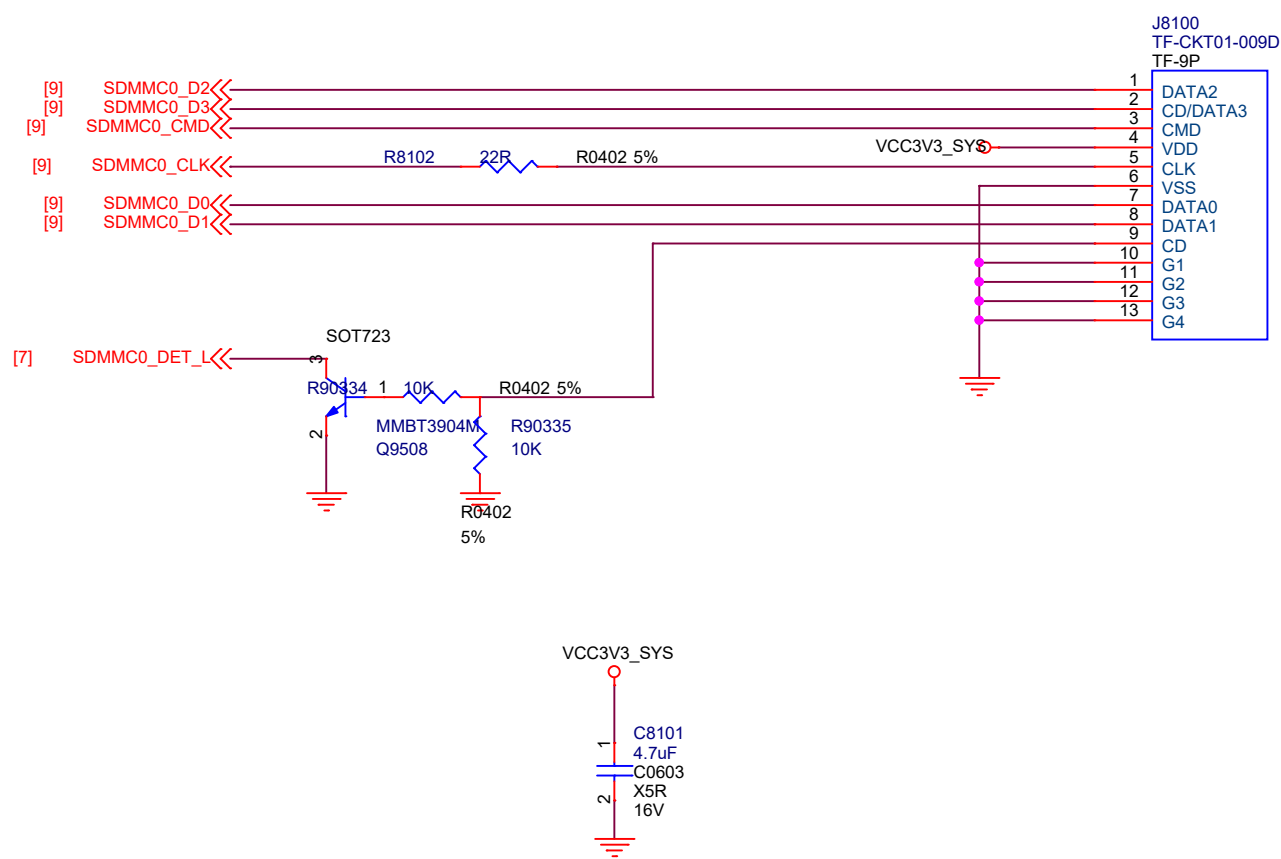
## eMMC NC PIN FOR ALLEGRO



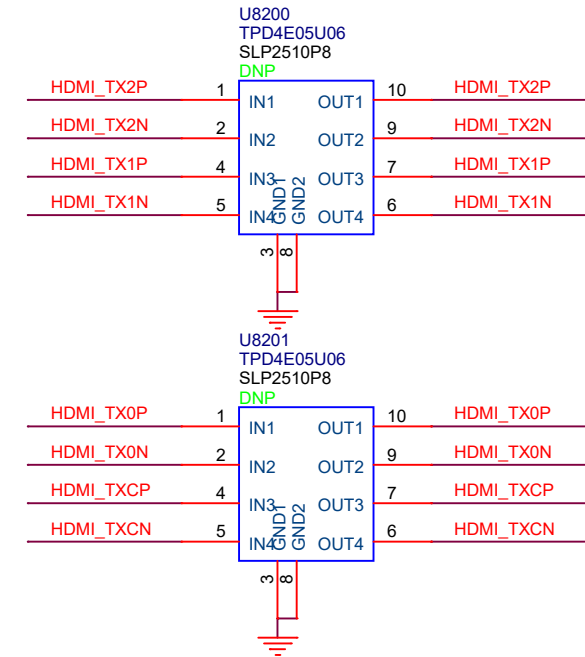
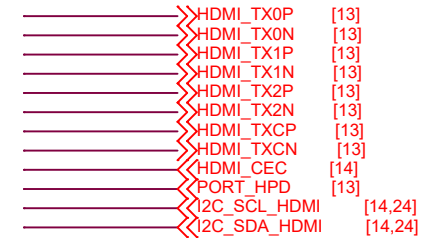
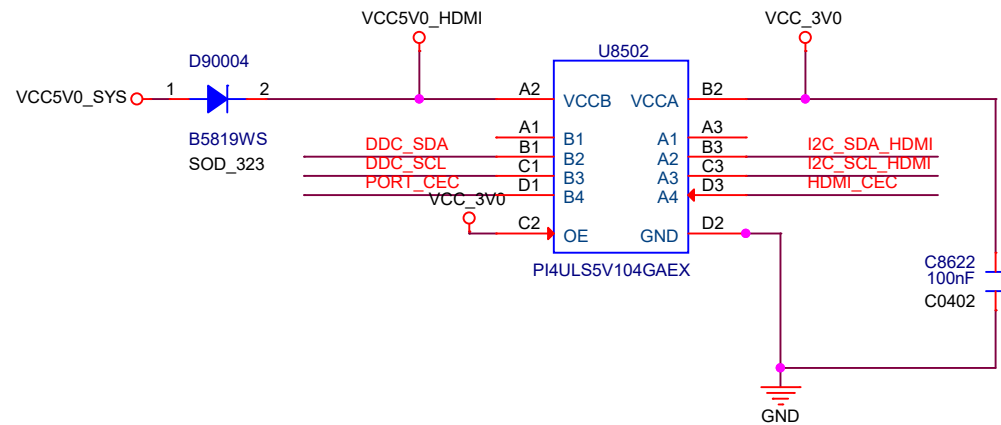
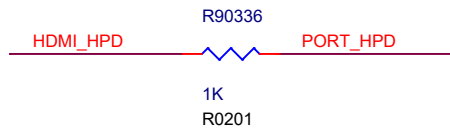
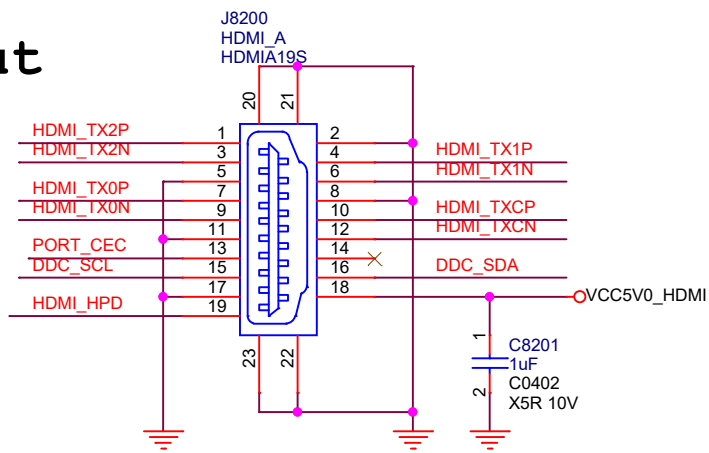
- SDIO0\_D0 [14]
- SDIO0\_D1 [14]
- SDIO0\_D2 [14]
- SDIO0\_D3 [14]
- SDIO0\_CMD [14]
- SDIO0\_CLK [14]
- UART0\_RTS [14]
- UART0\_TXD [14]
- UART0\_RXD [14]
- UART0\_CTS [14]
- BT\_HOST\_WAKE\_L [7]
- BT\_WAKE\_L [14]
- BT\_REG\_ON\_H [7]
- WIFI\_REG\_ON\_H [7]
- WIFI\_HOST\_WAKE\_L [7]
- RTC\_CLKO\_WIFI [17,22]



TF CARD



## HDMI Output

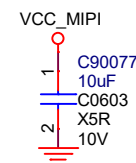
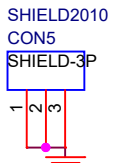
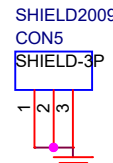
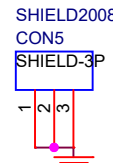
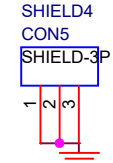
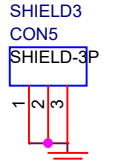
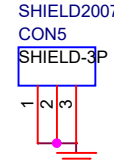
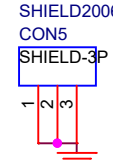
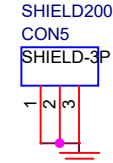
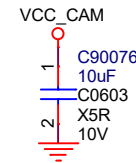
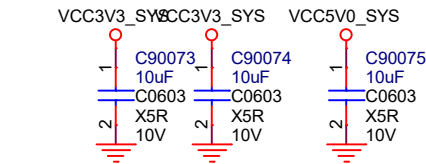
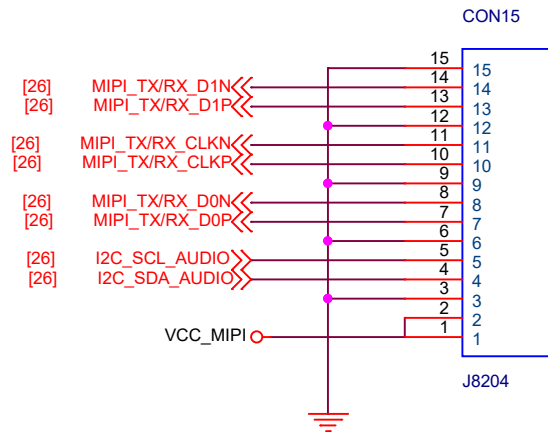
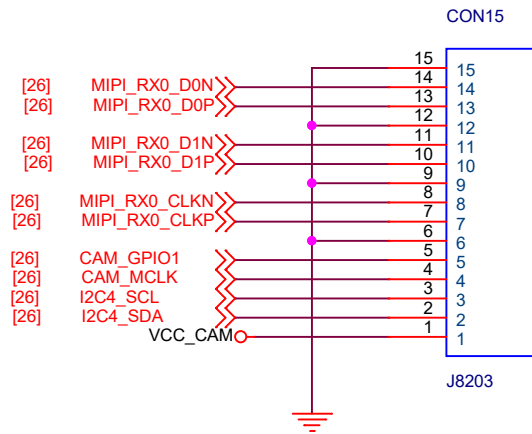
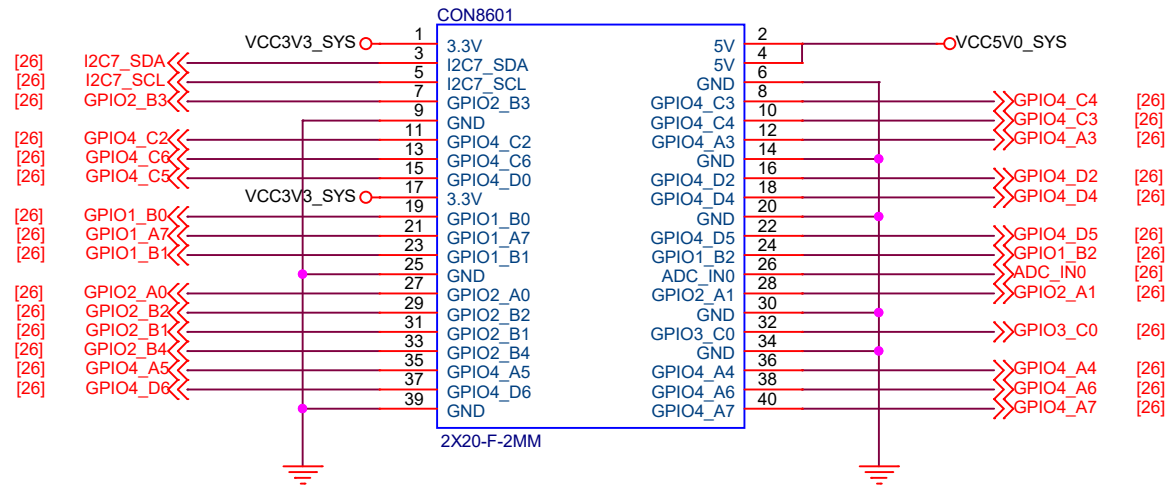


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A4	Page Name: HDMI Output	1.72
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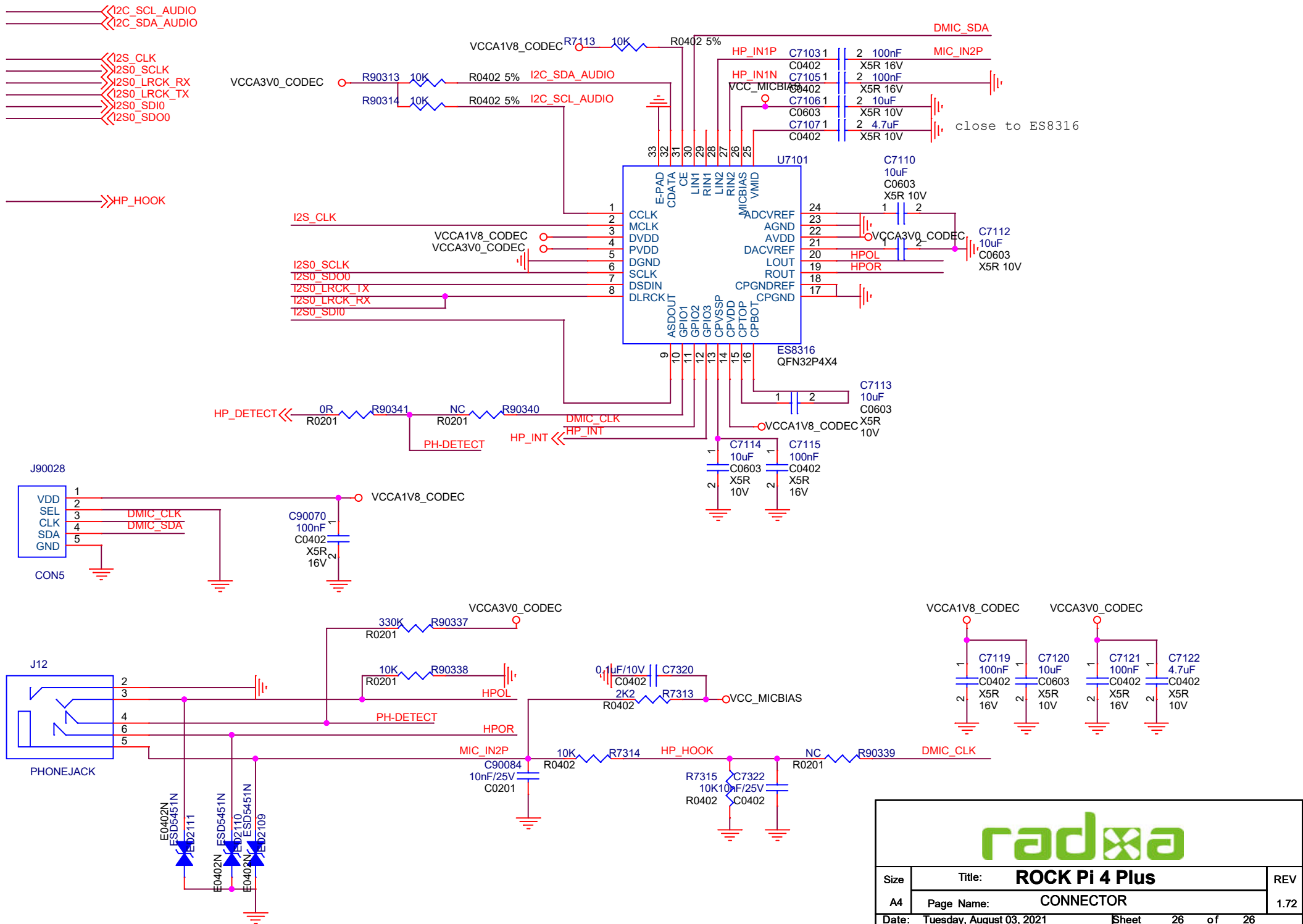


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File:	<Page name>			
Date:	Thursday, June 24, 2021	Rev:	V1.0	
Designed by:	<designer>	Sheet:	26 of 26	



radxa

Size	Title: <b>ROCK Pi 4 Plus</b>	REV
A4	Page Name: <b>CONNECTOR</b>	1.72
Date: Tuesday, August 03, 2021	Sheet 26 of 26	